

# The Impact of PLC-to-DSL Interference on VDSL2, Vectored VDSL2, and G.fast

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**Abstract**—This contribution presents an analysis of the impact of PLC-to-DSL interference on three wideband DSL technologies: VDSL2, Vectored VDSL2 (V-VDSL2), and G.fast. The impact was assessed via computer simulation, but measured loop responses and measured FEXT were also used together with a large set of PLC interference measurements collected from a large number of residential inside wires. The impact of PLC-to-DSL interference on the achievable data rate is assessed at various loop lengths. We have found that the impact of PLC interference on DSL is small on short loops but it grows quickly as loop length increases. We have also confirmed that the use of vectoring greatly increases the sensitivity to PLC interference of DSL technologies, as vectoring removes the time-invariant “blanket” of crosstalk and leaves DSL exposed to PLC interference as well as to other alien noise.

## I. INTRODUCTION

Over the past two decades, broadband access technologies have seen an increasing level of sophistication across a variety of media, allowing consumers to enjoy an unprecedented growth in access speed [1]. The most widespread broadband technology in the world is a family of technologies that provides broadband access over the local telephone network, i.e. Digital Subscriber Line (DSL). Roughly two-thirds of all broadband subscribers worldwide are DSL subscribers, and there are more new DSL subscribers each month than new subscribers for all other access technologies combined.

The most recent DSL technologies being deployed today by operators are Very-high rate Digital Subscriber Line (VDSL2) [2] and V-VDSL2 [3]. Both VDSL2 and V-VDSL2 operate on frequencies up to 17 MHz or 30 MHz. The latest DSL technology that has been standardized in the ITU-T is G.fast (Fast Access to Subscriber Terminals) [4]. G.fast aims at providing ultra-high speeds over copper twisted pairs up to and sometimes even exceeding speeds of 1 Gbps and at a distance ranging between 50 to 250 meters. G.fast uses vectoring to cancel self-FEXT and is being specified over frequencies up to 106 MHz [5].

As the speed of access technologies keeps growing, home networking technologies will have to keep up in terms of data rate. A good candidate for high speed home networking is Power Line Communication (PLC) as it leverages the existing power cables in the home and has today reached a good technological maturity [6], [7]. Up to a few years ago, PLC data rates of several hundred Mbps were available using technologies based on the IEEE 1901 Broadband Powerline

Standard [8] and the ITU-T G.hn standard [9]. Recently, PLC technologies using frequencies up to 100 MHz with MIMO capabilities have also been introduced, e.g. HomePlug AV2 [10] and the ITU-T MIMO G.hn [11]. These advanced PLC technologies achieve data rates up to 1 Gbps [12].

Since the overlap in the frequency bands used by DSL and PLC is increasing, the issue of EMC naturally arises. Furthermore, the new vectoring capabilities of the most recent DSL technologies makes DSL more susceptible to PLC interference (as well as to any other in-home noise) because the time-invariant “blanket” of crosstalk that once covered most in-home noises is now gone thanks to vectoring. The issue of whether PLC can create harmful interference to DSL or not has been addressed for example in [13]–[18]. The goal of these studies was mostly to understand the general effect of PLC interference on DSL, especially its dependency on cable topologies (e.g., length, separation, load, twisting) and the effectiveness of interference mitigation techniques. However, to the best of the Authors’ knowledge, statistical models on PLC-to-DSL interference are not publicly available and the impact of PLC interference on DSL has not yet been assessed.

In the present work, we leverage a vast measurement campaign on PLC-to-DSL interference to analyze in detail the effects of measured PLC-to-DSL interference on three important DSL technologies: VDSL2, V-VDSL2, and G.fast. In a companion paper, we also derive a statistical model for the PLC-to-DSL interference [19]. These results were presented in March 2014 at the ITU-T Study Group 15 DSL standardization Working Group [20].

Achieving a good understanding of the impact that BB-PLC interference may have on DSL is important today as proposals for relaxing the PLC PSD above 30 MHz are currently being discussed in CENELEC. The simulation results presented here as well as the statistical model presented in [19] provide the necessary tools for carrying out an objective assessment of the impact that BB-PLC may have on the various DSL technologies.

## II. MEASUREMENT CAMPAIGN

Couplings were measured between existing in-home power lines and telephone inside wire at many different single-family homes and apartments in France.

An Arbitrary Waveform Generator (AWG) was used as a PLC transmitter, and a baseband signal with a -60 dBm/Hz PSD and a 125 MHz band was continuously injected in the power line socket by means of a passive coupler with good wideband characteristics in the 1-100 MHz band. The PLC-to-DSL interference coupled onto the customer's telephone copper pairs is measured with a digital oscilloscope sampling at 250 Msamples/s and connected via an impedance matching balun to a phone socket. Each time-domain trace contained 25 million samples, corresponding to a duration of 100 ms. Also the noise present on the phone wires in the absence of PLC interference was measured (baseline noise).

Further processing on the time-domain waveforms was performed to estimate the PSD of the baseline noise and the PLC-to-DSL interference couplings. A modified Welch algorithm was used to estimate the noise PSD at a phone socket and couplings were then computed by subtracting the excitation signal injected by the AWG. The resulting couplings were spline-interpolated to extract couplings lying on the DSL frequency grid of 4.3125 kHz or its multiples.

In this work, a total of 240 time-domain PLC-to-DSL interference traces were collected where each measurement represents a coupling realization between a power line outlet and a phone socket in the same house/apartment. Also a total of 44 time-domain ambient noise traces on twisted-pairs were collected at each location in the absence of PLC-to-DSL interference (baseline noise). A total coupling population of approximately 3.1 million samples were used in this work.

It is well known that the PLC channel is time-varying [21]. Recently it has also been pointed out that the broadband PLC channel is actually a Linear and Periodically Time-Varying (LPTV) channel and is thus amenable to being represented with a Zadeh decomposition [22], [23]. Since the PLC channel is LPTV, then one would expect that also PLC-to-DSL interference is periodically time-varying as well.

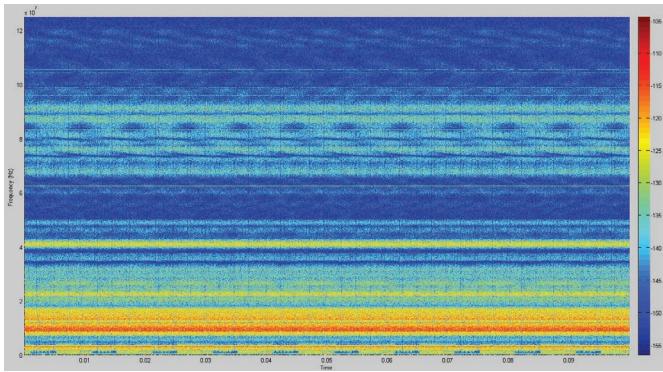


Figure 1: Spectrogram of one PLC-to-DSL interference realization. Time is in seconds (from 0 to 0.1 s) and frequency is in Hertz (from DC to 125 MHz).

This conjecture can be verified by looking at the spectrogram of the noise observed on a twisted-pair when the PLC signal is present on the power cables. The spectrogram of one PLC-to-DSL interference realization is shown in Figure 1. It is easy to notice that, although most frequency components

of the channel are static over time, there are clearly some frequency components that change every 10 ms (half of the mains period of 1/50 Hz) and typically assume two values. This confirms (indirectly) that the PLC channel is indeed LPTV, but also confirms for the first time that also the induced PLC-to-DSL interference has an LPTV nature. By performing PSD estimation via the Welch algorithm, we arrive at an estimate of the PSD of the noise/interference signal which will be an “average” PSD, i.e. each frequency component of the PSD will assume a value that is the time average of the spectrogram along the time-axis. The Welch estimate of the PSD of the signal used to create the spectrogram is showed in Figure 2. This average PSD is used to extract the PLC-to-DSL interference couplings

Further details of this measurement campaign can be found in a companion paper [19].

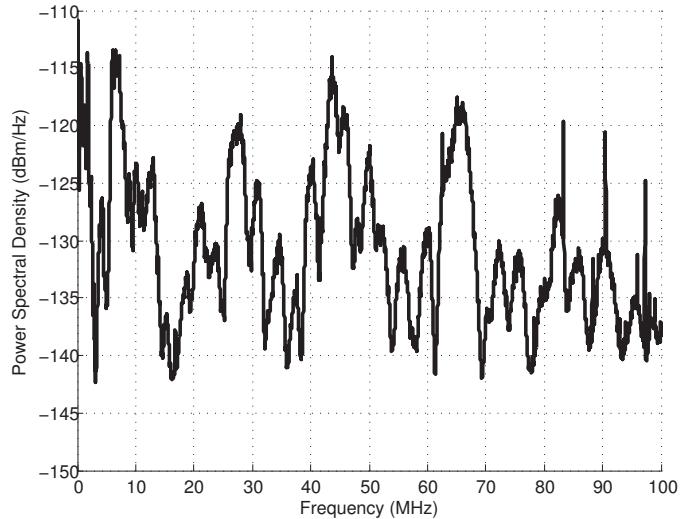


Figure 2: Estimated PSD of the PLC interference signal used to create the spectrogram in Figure 1.

### III. SIMULATION METHODOLOGY

#### A. PLC Interference

Realizations of PLC-to-DSL interference were generated using the couplings estimated from the measurements. PLC interference was generated assuming a maximum allowed PSD of -55 dBm/Hz from 2 to 30 MHz and of -85 dBm/Hz between 30-87 MHz, while no PLC transmission is present in the FM broadcast band of 87-100 MHz. This choice is consistent with IEEE 1901 [8], HomePlug AV2 [7], and ITU-T G.hn [9]. This transmit PSD is added, in dB, to the estimated couplings to form a realization of the noise PSD for the DSL downstream receiver. This methodology assumes that the PLC node is continuously transmitting, and this is a worst case scenario. This was done for each of the 240 measurements and statistics of bit rate were generated and compared to the case with no PLC interference and only measured baseline noise present.

### B. VDSL2 and V-VDSL2

VDSL2 uses high frequencies and loop lengths typically up to 1.5 km to transmit at speeds of at most a few hundred Mbps. VDSL2 uses frequency-division duplexing, upstream and downstream, to avoid near-end crosstalk (NEXT). However, VDSL2 can still be limited by far-end crosstalk (FEXT) which causes VDSL2's data rates to drop in dense deployments.

Vectoring greatly improves the performance of VDSL2 as it removes the FEXT created within a vectored group by performing precoding at the transmitter (downstream) and crosstalk cancellation at the receiver (upstream). Thus, vectoring allows maintaining the VDSL2 data rate of a few hundred Mbps regardless of the number of self-closers.

The simulations here calculate downstream VDSL2 bit rates. The simulations generally use models and parameters from ANSI Std. T1.413 [24], including the BT loop model. VDSL2 Profile 17a is simulated, and the transmit PSD is at most 3.5 dB below the VDSL2 profile 998ADE17-M2x-A PSD limit mask defined in Annex B of G.993.2 [2]. Additionally, the maximum transmit PSD is limited to meet the G.993.2 average power constraint and there is no DPBO. For VDSL2 data rate calculations, there are two worst case FEXT disturbers. For V-VDSL2, the simulations model the ideal case of complete in-domain crosstalk cancellation and no out-of-domain/alien crosstalk present [25]. The measured baseline noise is added to the received signal at each receiver.

For the downstream data rate calculation, the margin is 6 dB and the total coding gain is 3 dB. Bit rates are calculated by summing the capacity calculation of each 4.3125 kHz tone with a 9.75 dB SNR gap, with bits per Hz per tone lower limited to at least one bit and upper limited to 14 bits per Hz per tone. A guard-band of 12 tones is imposed between each passband and these guard-bands carry no bits. Loops are all 0.5mm/24 AWG. VDSL2 has 10% overhead, all presented data rates are net of this overhead.

### C. G.fast

G.fast was simulated with linear zero-forcing precoders and the following typical assumptions:

- DMT with 2048 carriers equally spaced between DC and 106 MHz.
- The transmit frequency band was from 2.5 MHz up to 106 MHz.
- The loop response and FEXT were based on a set of measurements reported by BT on a 100m distribution cable [26]. For shorter/longer lengths, the magnitude of the response is scaled linearly (in dB) with length.
- A full cable of 10 active and vectored lines was simulated.
- Vectoring is performed using linear zero-forcing precoders. No channel estimation is performed (perfect knowledge of the channel matrix is assumed at the transmitter) and there is no precoder quantization error.
- The G.fast PSD is always normalized, so that the transmit PSD is unaltered by precoding at all frequencies.
- The G.fast PSD is limited as in Recommendation ITU-T G.9700, with PSD mask of -65 dBm/Hz below 30 MHz,

and linearly sloping from -73 dBm/Hz at 30 MHz down to -76 dBm/Hz at 106 MHz. This is further limited to meet the 4.0 dBm total transmit power limit by limiting the max transmit PSD to -76.15 dBm/Hz when transmitting from 2.5 to 106 MHz.

Data rate is calculated by summing the capacity of each 51.75 kHz G.fast sub-carrier with a 9.75 dB SNR gap, with bits per Hz lower limited to at least one bit per Hz and upper limited to 12 bits per Hz. Margin was set to 6 dB and total coding gain to 3 dB. Differently from the VDSL2 and vectoring cases, speeds of G.fast are maximum total line rate<sup>1</sup>. Presented data rates are raw line rates, i.e. overhead has not been accounted for.

Since measured cable responses and FEXT were used, then the direct and crosstalk channels are different from line to line and this leads to variation in bit rates between lines even when no PLC-to-DSL interference is present. Furthermore, the linear precoder amplifies the signal power at high frequency where the crosstalk is much stronger than at lower frequency making the channel matrix not row-wise dominant as it would be when upper frequencies are limited to about 30 MHz.

## IV. SIMULATIONS RESULTS

The simulations presented in this section calculate data rate losses, where this loss is between the case when PLC is off (only baseline noise present) and when PLC is on. AWGN at -140 dBm/Hz is also added in all cases.

### A. VDSL2

Simulations were run with two 99% worst-case self-FEXT disturbers [24], and results of non-vectored VDSL2 downstream data rates are shown in Figure 3. We can notice that, for short loop lengths, the SNR decrease due to PLC interference is very small and does not cause much impact, while at longer loop lengths the effects are more severe. This can be explained by the fact that FEXT "covers" PLC interference and FEXT strength decreases with distance.

Figure 4 shows the Complementary Cumulative Distribution Function (C-CDF) of the percent decrease of VDSL2 bit rates caused by PLC interference, with respect to the case where FEXT and baseline noise are present. The Kaplan-Meyer estimate of the empirical CDF was used here. The Figure is useful for assessing what the probability of having a data rate decrease of at least a certain percentage is, with respect to the case when no PLC interference is present. For example, a data rate loss of 10% or more can occur with a probability of 0.02 at 300m, while on shorter loop lengths the impact suffered by VDSL2 is negligible. The C-CDF plot clearly shows that the probability of moderate to substantial VDSL2 data rate degradation due to PLC interference is very small on loops shorter than a couple of hundred meters but then grows as loop length increases.

<sup>1</sup> Unlike previous DSL standards, G.fast uses Time Division Duplexing (TDD) and the asymmetry ratio can be varied. Rather than arbitrarily picking an asymmetry ratio, we used the maximum data rate (upstream plus downstream) as if 100% of resources were devoted to downstream.

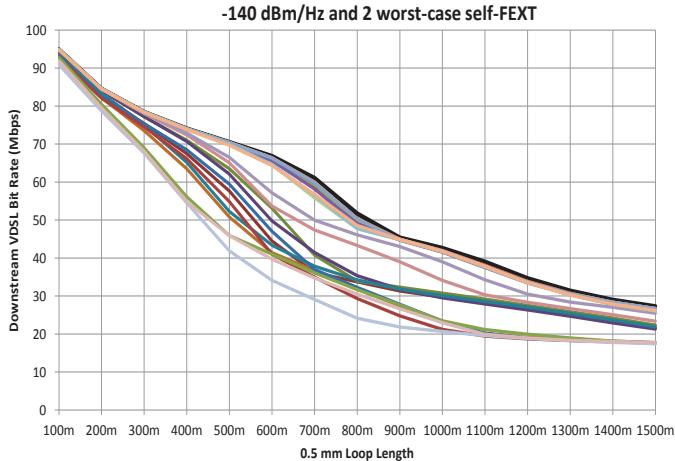


Figure 3: Downstream VDSL2 bit rates with two worst-case self-FEXT disturbers. The top bold black curve is the data rate achieved in the absence of PLC interference. Only 25 of the 240 PLC interference realizations are shown.

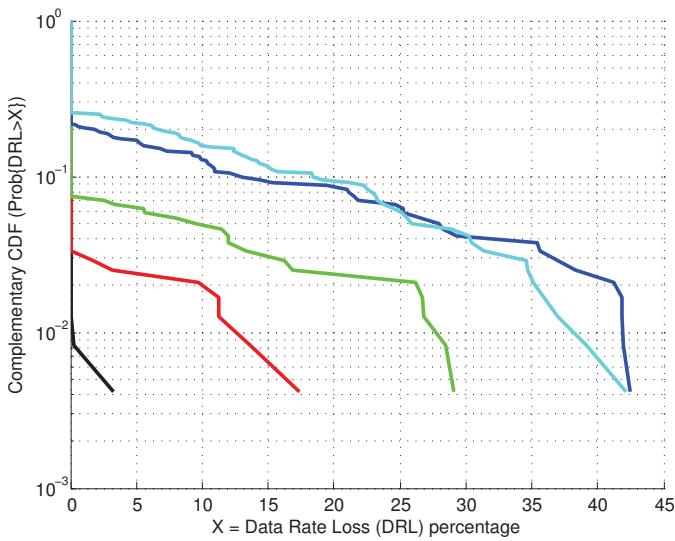


Figure 4: C-CDF of percent decrease in VDSL2 downstream bit rates caused by PLC interference for the case of two worst-case self-FEXT plus baseline noise. From left to right, loop lengths of 200, 300, 400, 600, 1,000 m.

The average and maximum VDSL2 data rate loss (with respect to the case of FEXT plus baseline noise) are plotted (in black) versus distance in Figure 5. Both average and maximum data rate loss take moderate values confirming the resiliency of VDSL2 to PLC-to-DSL interference.

#### B. Vectored VDSL2

For the case of vectoring, the time-invariant “blanket” of crosstalk is removed leaving the DSL system much more exposed to alien noise, including PLC interference. Thus, we expect a higher probability of degradation for V-VDSL2 than for non-vectored VDSL2, and even for short loops. This intuition is confirmed by our simulations.

In Figures 6, the downstream data rates of V-VDSL2 impaired by PLC interference are shown versus loop length.

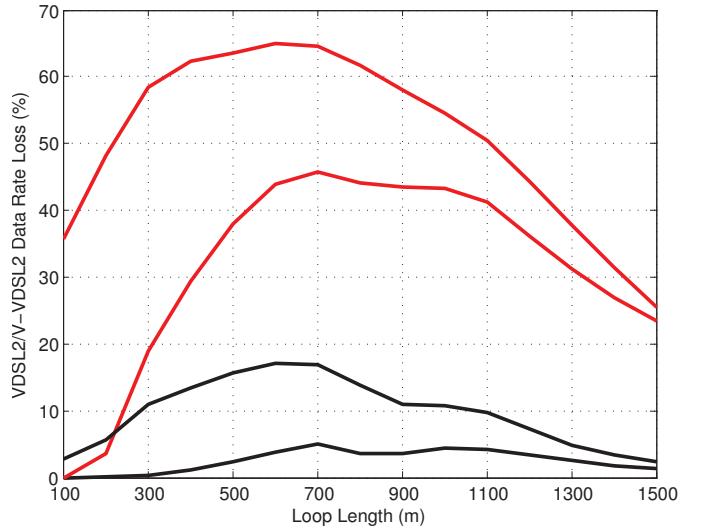


Figure 5: Average and maximum data rate loss (percentage) versus distance for VDSL2 (black) and V-VDSL2 (red).

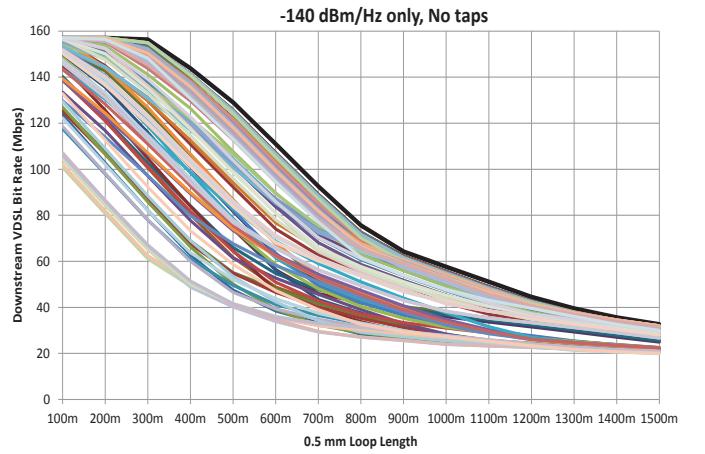


Figure 6: Vectored VDSL2 data rates. The top bold black curve is the achieved data rate in the absence of PLC interference. Only 25 of the 240 PLC interference realizations are shown.

Data rate degradation is not only more substantial compared to the non-vectored VDSL2 case, but it also occurs substantially at all loop lengths.

The C-CDF of the percent decrease of vectoring bit rates was computed on the basis of the Kaplan-Meyer estimate of the empirical CDF and it is shown in Figure 7. The probability of degradations is now much higher than in the previous non-vectored case. For example, a data rate loss of 10% or more can occur with a probability of 0.1 at 100m, and this probability increases to 0.35 (0.45) when the loop length is 300m (500m). In another example, there is a probability of 0.05 to observe a data rate loss of at least 20% at 100m, 32% at 200m, and 54% a 500m.

The average and maximum V-VDSL2 data rate loss are plotted (in red) versus distance in Figure 5. The meaningful range for V-VDSL2 is up to 500 m and, in this range, both average and maximum data rate loss grow quickly with

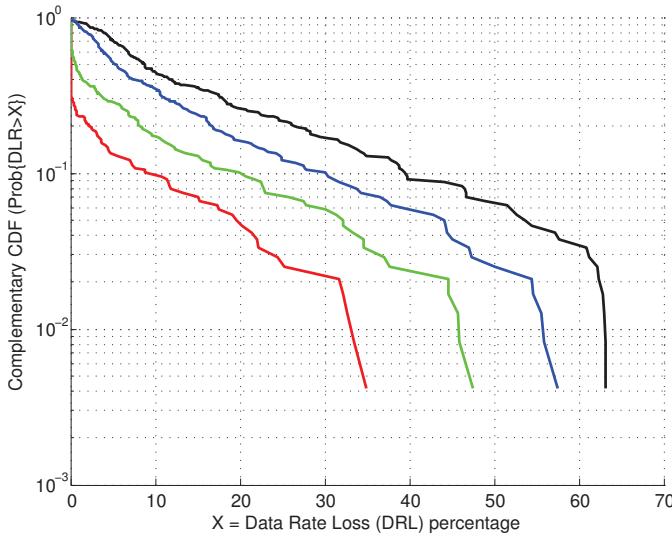


Figure 7: C-CDF of percent decrease in V-VDSL2 (no self-FEXT) downstream bit rates caused by PLC interference. From left to right, loop lengths are 100, 200, 300, and 500 m.

distance and can be large. This confirms the sensitivity of V-VDSL2 to PLC-to-DSL interference.

### C. G.fast

We have evaluated the performance of a G.fast system on the basis of real loop and FEXT measurements. The 240 available PLC-to-DSL interference realizations were used for the calculation of the data rates of 10 G.fast vectored lines, allowing the use of 24 different realizations per line. Similarly, the G.fast data rates achieved in the presence of measured baseline noise only were also calculated.

The average (across both G.fast lines and measured interference realizations) data rates versus loop length in the presence of AWGN, measured baseline noise, and measured PLC-to-DSL interference are shown in Figure 8. The maximum and minimum average data rate achieved across the 10 G.fast lines are also plotted. For every G.fast line, 24 data rate losses were calculated (from the data rate of G.fast lines affected by measured baseline noise only to the data rate of G.fast lines in the presence of measured PLC-to-DSL interference) and their histogram is shown in Figure 9 for the two cases of loop length equal to 100m and 200m. The histogram value  $y(k)$  represents the normalized count of occurrences in the interval  $[x(k), x(k + 1))$ .

At the shorter 100 m loop length, nearly 60% of realizations of PLC-to-DSL interference yield degradation of only up to 1% to G.fast but the maximum data rate loss can be as high 40%. However, at the longer 200 m loop length, the situation is different and the G.fast data rate degradation appears more uniformly distributed. In particular, now only 15% of realizations yield an impact of 1% or less to G.fast, while the maximum data rate loss is 80%.

We have also looked at average and maximum decrease in data rate as a function of loop length. This is shown

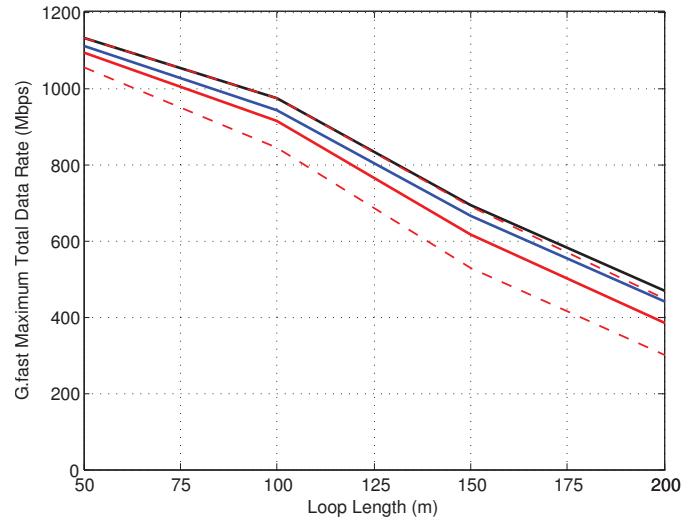


Figure 8: Average G.fast data rates versus loop length in the presence of AWGN at -140 dBm/Hz (solid black), measured baseline noise (solid blue), and measured PLC-to-DSL interference (solid red). The maximum and minimum average data rates achieved across the 10 G.fast lines when PLC-to-DSL interference is present are also shown (dashed red).

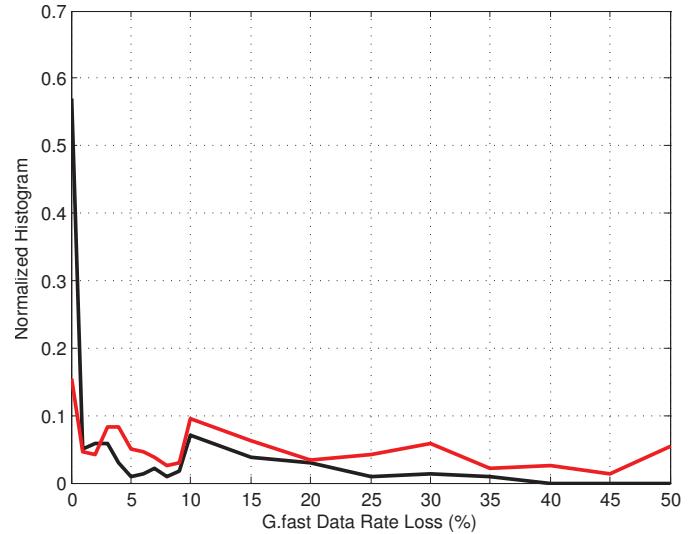


Figure 9: Histogram of G.fast percentage data rate losses for the cases of loop length equal to 100 m (black) and 200 m (red). The last histogram bin includes data rate degradations of 50% or more.

in Figure 10. Although, on the average, PLC interference induces a limited degradation on G.fast (and especially at short distances), there are cases when coupling between residential power and telephone wiring can be substantial and this can degrade G.fast data rates up to 80% depending on distance.

The modest average impact of PLC interference on G.fast may be explained by the fact that G.fast operates on very short loops where the SNR is high and that G.fast transmits at most 12 bits per Hz so that low to moderate levels of coupling between residential power and telephone cables have a negligible effect. We also point out that in these G.fast simulations vectoring is not ideal, so residual uncanceled FEXT is indeed

present. This residual crosstalk masks some PLC interference, and this contributes to making G.fast degradation small at short distances like in the VDSL2 case.

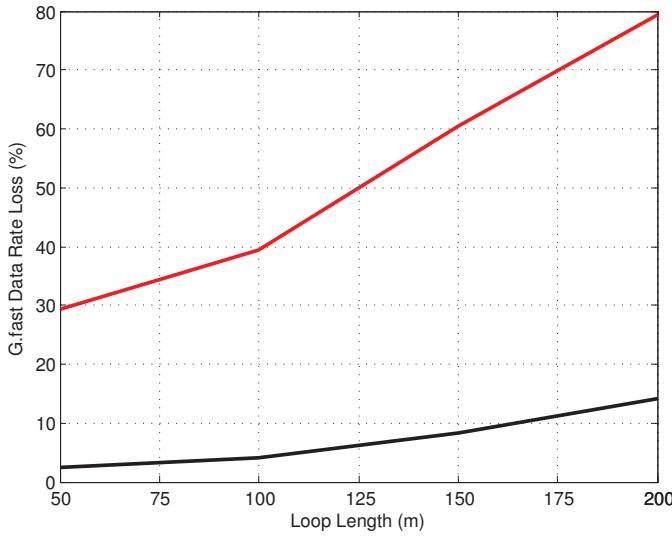


Figure 10: Average and maximum G.fast data rate loss (percentage) versus distance.

## V. CONCLUSIONS

The impact of PLC interference on DSL technologies is proportional to loop length and on whether vectoring is used or not, i.e. whether crosstalk is present or not. On very short loop lengths (less than a couple hundred meters), there is a high probability that the impact of PLC interference is small. For example, we have ascertained that the probability that V-VDSL2 suffers less than 20% data rate loss because of PLC interference can be as high as 95% at loop lengths of 100 m. However, this probability decreases to 75% and 60% at 300 m and 700 m, respectively. The impact of PLC interference on non-vectored VDSL2 is smaller because of the protective “blanket” of crosstalk that masks PLC interference.

As far as G.fast, which is specified to operate on very short loops and with vectoring, the impact of PLC-to-DSL interference is not dissimilar from the case of V-VDSL2. The average data rate loss of G.fast is small (from 2% to 14%, depending on distance) but, when the coupling between PLC and DSL is high, then the maximum data rate loss can be as high as 30%-80%.

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